Technical Note
DDR3 Termination Data Strobe (TDQS)

Introduction

To simplify memory controller design for systems that simultaneously use both x4-based and x8-based registered DIMMs, Micron® DDR3 provides the termination data strobe (TDQS) function. DIMMs that are x8-based only require one DQ strobe pair (DQS/DQS#) for each 8-bit byte; x4-based DIMMs require a DQS pair for each 4-bit nibble (a total of four strobe lines). When these two different DIMM configurations are mixed within the same system, the loading of the DQS lines differs. These loading differences can cause signal integrity issues.

TDQS is similar to the RDQS function in DDR2, however, TDQS provides only termination. RDQS provides both termination and an output strobe.

This technical note provides guidelines for using the TDQS feature to reduce signal-integrity issues associated with mismatched DQS loading in combined x4-based/x8-based systems.

TDQS Ball Assignment

TDQS is only available on x8 DRAM devices. TDQS is shared physically with the data mask (DM) ball and is an either/or function. TDQS# has a dedicated ball on the device that is not used if the TDQS function is disabled.

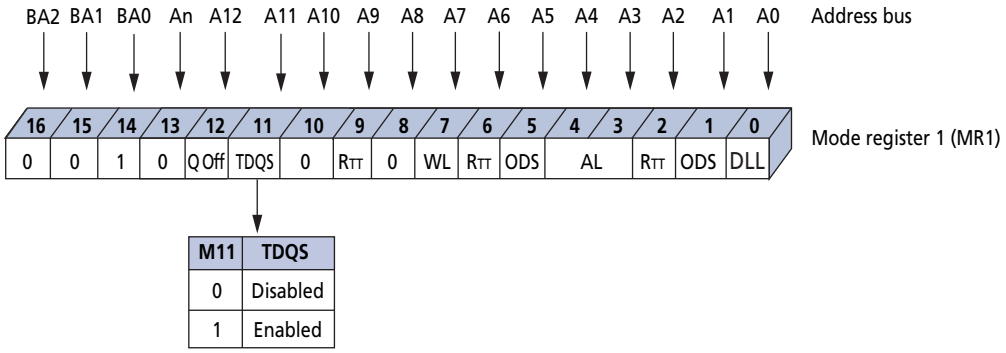
Table 1: TDQS/TDQS# Matrix

MR1[11] Setting	DM/TDQS Ball Function	NU/TDQS# Ball Function
0 (TDQS function disabled)	DM	High-Z
1 (TDQS function enabled)	TDQS	TDQS#

Functional Description

When enabled, TDQS provides termination on both the TDQS and TDQS# balls that is equal to the termination selected on DQS and DQS#. To enable the TDQS function on the DRAM, set MR1[11] to “1” (see Figure 1 on page 2). Using this setting, the upper nibble strobes from the x4-based DIMM have the same loading and termination as the lower nibble strobes even though they are not required for operation on the x8-based DIMM.

Figure 1: Mode Register 1 (MR1)



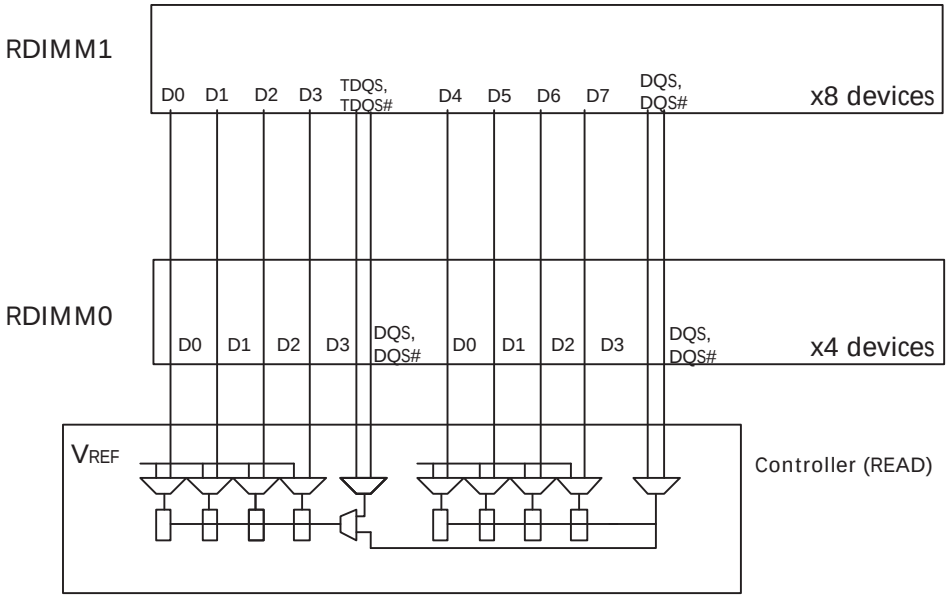
When TDQS is enabled via the mode register, the DM function is not supported. When TDQS is disabled, the DM function is provided and the TDQS# ball is not used. Because the TDQS function is only available on x8 configuration DRAM devices, for x4 and x16 devices, TDQS must be disabled in the mode register by setting MR1[11] to "0."

Example of TDQS Use

An example of a system using the TDQS function is shown in Figure 2 on page 3. In this 2-slot system, one slot is populated with an RDIMM design using x4 DRAM devices (RDIMM0); the other slot is an RDIMM using x8 devices (RDIMM1). The RDIMM populated with x4 devices requires two DQ strobe pairs for operation. One of these strobe pairs must be routed to RDIMM1 for proper functionality. The other strobe pair is not required for operation on RDIMM1; it is, however, routed to RDIMM1 and connected to the TDQS/TDQS# balls. When TDQS is enabled, this connection ensures that all of the strobe lines are loaded equally.

If TDQS is disabled, there will be two stubs with unequal loading and no termination. Lack of termination and differences in signal loading can cause timing and signal-integrity issues.

Figure 2: TDQS System Example



Summary

The TDQS feature on Micron DDR3 devices provides greater overall system flexibility. To compensate for signal integrity issues caused by mixing x4- and x8-configured DIMMS, connect the extra set of strobes from the x4 DIMM to the TDQS balls on the x8 DIMM and enable the feature in the mode register.

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